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Hardware-Algorithms Co-Design and Implementation of an Analog-to-Information Converter for Biosignals Based on Compressed Sensing. Pareschi F, Albertini P, Frattini G, Mangia M, Rovatti R, Setti G. We report the design and implementation of an Analog-to-Information Converter Hardware-Algorithms Co-Design and Implementation of an ...

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Hardware design: Adopting increasingly accurate and robust algorithms often increases computational complexity and, hence, needs a powerful hardware platform to implement these algorithms. It, in turn, requires us to further improve both system architecture and circuit implementation in order to boost the computing power for real-time operation.

Algorithm and hardware implementation for visual ...

The theme of the System Chip Design Laboratory is algorithms into hardware. This theme captures the concept that signal and data processing executing sequentially on a conventional device can be enhanced by the unique vector and parallel processing capabilities of the field programmable gate array (FPGA).

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Algorithms into Hardware – System Chip Design Laboratory

In this post we are going to find out the Step By Step implementation of AES-128 bit algorithm on FPGA/ASIC platform using Verilog language. It has been divided in two sections, i.e. Background and...

AES algorithm and its Hardware Implementation on FPGA- A ...

FPGA based hardware implementation of Bat Algorithm Graphical abstract
Mohamed Sadok BEN AMEUR(1,2), Anis SAKLY(2), 1: Laboratory of Electronic and Microelectronic, University of Monastir, Tunisia. Mohamed sadok ben ameur, msba2014@gmail.com 2: Research unit ESIER, National Engineering School of Monastir, University of Monastir, Tunisia. Anis sakly, Sakly_anis@yahoo.fr,

FPGA based hardware implementation of Bat Algorithm

Star tracker is the most accurate attitude sensor that determines satellite direction by applying centroiding algorithm, star identification and attitude determination. To utilize such algorithms, first, high quality of star images are needed which should be provided through the star tracker camera.

Modification and hardware implementation of star tracker ...

Hardware-Algorithms Co-Design and Implementation of an Analog-to-Information Converter for Biosignals Based on Compressed Sensing. Pareschi F, Albertini P, Frattini G, Mangia M, Rovatti R, Setti G. We report the design and implementation

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of an Analog-to-Information Converter

Hardware-Algorithms Co-Design and Implementation of an ...

In hardware implementation of CRC algorithms such as in software implementation the parametric model can be changed by changing Poly, Init, Refln, ReflnOut, XorOutparameters. However unlike a software implementation in hardware each parameter requires I/O FPGA pins which prevent parametric model control.

A study of hardware implementations of the CRC computation ...

Both digital and analog hardware implementations of bead sort can achieve a sorting time of $O(n)$; however, the implementation of this algorithm tends to be significantly slower in software and can only be used to sort lists of positive integers. This is a perfect example of an algorithm where the hardware implementation is significantly faster than the software implementation is to contrary to the common belief that software has to be faster than corresponding hardware (think of mechanical ...

Bead Sort: An algorithm that works faster with hardware ...

space. Thus, software implementation has great difficulties. In contrast, hardware encryption has high security, fast speed and strong real-time property. At present, FPGA-based RSA hardware encryption and decryption is a new research direction, and an improved study on the existing low-radix Montgomery algorithm has been

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made in this article.

Improvements of RSA algorithm for hardware encryption ...

Hardware implementation. The schematic for hardware implementation based upon the NSE real-time software algorithm (spectral_estimate_real_time) is shown in Figure 6. The hardware consists of a mix of analog and digital components, and for simplicity it is shown as sampling the data at exactly 1.0 kHz (1 millisecond intervals) using a 1 kHz clock.

Software algorithm and hardware design for real-time ...

efficient hardware and/or software physical implementation. Based on the experience accumulated in the process of implementing a segmentation algorithm, this thesis outlines a design for implementation methodology comprised of a development flow and associated

Design for Implementation of Image Processing Algorithms

October 25th, 2018 - By: John Swanson. Petabytes of data efficiently travels between edge devices and data centers for processing and computing of AI functions. Accurate and optimized hardware implementations of functions offload many operations that the processing unit would have to execute. As the mathematical algorithms used in AI-based systems evolve, and in some cases stabilize, the demand to implement them in hardware increases, freeing compute

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resources.

Implementing Mathematical Algorithms In Hardware For ...

Abstract- This paper describes the hardware implementation methodologies of fixed point binary division algorithms. The implementations have been extended for the execution of the reciprocal of the binary numbers. Radix-2 (binary) implementations of digit recurrence and multiplicative based methods have been considered for comparison.

HARDWARE IMPLEMENTATION OF METHODOLOGIES OF FIXED POINT ...

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New algorithms (elliptic curves) may reduce application complexity, but still designers must wrestle with the trade-offs between implementing security in software or hardware. Although there will always be exceptions for specific services, niche markets, or very small chips, embedded cryptography is replacing software cryptography for a wider range of services.

Cryptography in Software or Hardware - It - Maxim Integrated

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The other implementation of a hardware-accelerated module is a hardware peripheral. Instead of passing data to a software function, you write data to a memory-mapped hardware peripheral. The computation is done outside of the CPU so the CPU can continue running code while the peripheral is working.

Accelerating algorithms in hardware - Embedded.com

In computer systems, an algorithm is basically an instance of logic written in software by software developers, to be effective for the intended "target" computer(s) to produce output from given (perhaps null) input. An optimal algorithm, even running in old hardware, would produce faster results than a non-optimal (higher time complexity) algorithm for the same purpose, running in more

...

The subject of this book is the analysis and design of digital devices that implement computer arithmetic. The book's presentation of high-level detail, descriptions, formalisms and design principles means that it can support many research activities in this field, with an emphasis on bridging the gap between algorithm optimization and hardware implementation. The author provides a unified view linking the domains of digital design and arithmetic algorithms, based on original formalisms and hardware description languages. A feature of the book

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is the large number of examples and the implementation details provided. While the author does not avoid high-level details, providing for example gate-level designs for all matrix/combinational arithmetic structures. The book is suitable for researchers and students engaged with hardware design in computer science and engineering. A feature of the book is the large number of examples and the implementation details provided. While the author does not avoid high-level details, providing for example gate-level designs for all matrix/combinational arithmetic structures. The book is suitable for researchers and students engaged with hardware design in computer science and engineering.

This dissertation deals with the design of high-speed, bilinear algorithms for digital signal processing applications that are especially suited for implementation on dedicated hardware platforms. Bilinear algorithms exhibit a high degree of concurrency as all multiplication operations involved are independent of each other and can be computed at the same time. Consequently, the critical path delay for hardware implementations of these algorithms is very low. The algorithms developed here have other important properties such as a well defined recursive structure, modularity and low complexity. The first two properties are important for efficient mapping of the algorithm onto hardware and the last property helps in reducing hardware cost. Bilinear algorithms also have the advantage that two or

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more smaller algorithms can be used to obtain a larger, composite algorithm.

The main objective of this thesis is the comprehensive analysis and synthesis with the hardwired square-rooting, believed to be the first subject to be implemented among various functions which are being evaluated mostly in software at present. Two new efficient algorithms for hardwired square-rooting, here called the algorithm G and algorithm T, have been developed and presented in the most detail. These use multiplication and no division. Furthermore, algorithm G possesses the property of quadratic convergence, a very important one for the machine of large word length as far as speed is concerned. Algorithm T is suitable for the machine of medium word length. (Author Modified Abstract).

Software-based cryptography can be used for security applications where data traffic is not too large and low encryption rate is tolerable. But hardware methods are more suitable where speed and real-time encryption are needed. Until now, there has been no book explaining how cryptographic algorithms can be implemented on reconfigurable hardware devices. This book covers computational methods, computer arithmetic algorithms, and design improvement techniques

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needed to implement efficient cryptographic algorithms in FPGA reconfigurable hardware platforms. The author emphasizes the practical aspects of reconfigurable hardware design, explaining the basic mathematics involved, and giving a comprehensive description of state-of-the-art implementation techniques.

A comprehensive evaluation of information security analysis spanning the intersection of cryptanalysis and side-channel analysis Written by authors known within the academic cryptography community, this book presents the latest developments in current research Unique in its combination of both algorithmic-level design and hardware-level implementation; this all-round approach - algorithm to implementation - covers security from start to completion Deals with AES (Advanced Encryption standard), one of the most used symmetric-key ciphers, which helps the reader to learn the fundamental theory of cryptanalysis and practical applications of side-channel analysis

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